

# A NOVEL MEMS SILICON PROBE CARD

Bong-Hwan Kim<sup>1,2</sup>, Sangjun Park<sup>1,2</sup>, Byeungleul Lee<sup>1</sup>, Jong-Ho Lee<sup>1,3</sup>, Bong-Gi Min<sup>4</sup>,  
Soon-Don Choi<sup>4</sup>, Dong-il (Dan) Cho<sup>1,2</sup>, and Kukjin Chun<sup>1,2</sup>

<sup>1</sup>School of Electrical Engineering, Seoul National University ENG420-038, Kwanak P.O. Box 34, Seoul 151-744, KOREA

<sup>2</sup>IC-MEMS, Inc., Interuniversity Semiconductor Research Center (ISRC), Seoul National University,  
San 56-1, Shinlim-dong, Kwanak, Seoul 151-742, KOREA

<sup>3</sup>School of Electrical, Electronic and Information, WonKwang University, 344-2 Shinyong, Iksan Chonbuk 570-749, KOREA

<sup>4</sup>School of Metallurgical and Materials, YeungNam University, 214-1, Dae-Dong, Kyongsan, Kyongbuk 712-749, KOREA  
Tel: 82-2-885-0647, Fax: 82-2-885-0648, e-mail: bhkim@ic-mems.com

## ABSTRACT

We have developed a novel cantilever-type probe which is capable of less than 70  $\mu\text{m}$  of pitch and 12g of force. This probe is suitable for wafer-level burn-in testing, function testing and circuit-board O/S testing including memory and RF devices. The probe was fabricated with epitaxial polysilicon on silicon substrate. The through via hole interconnection was formed in silicon wafer by nickel electroless plating and copper electroplating. The electroless plating is easy method and can deposit film uniformly for deep trench and through hole. Especially, it can deposit film on any substrates without seed layer and allow it to be electroplated. The aspect ratio of through via hole was larger than 10:1 and the contact resistance was less than 1 ohm.

## INTRODUCTION

It is the most challengeable work to achieve reliable, efficient, and cost-effective probe for IC test. The implementation of high performance probe becomes difficult with the conventional technology, because the number of pads per die increases and the pitch between pads decreases. The epoxy ring probe card, long the industry standard for probing silicon wafer, continues to dominate as the principal interface between the wafer and ATE (Automatic Test Equipment) as shown in Fig. 1. The conventional epoxy-type probe card consists of a PCB (printed circuit board) that supports an array of delicate wire contacts. These contacts serve as the electromechanical interface between the device under test, so-called DUT, and the test electronics [1]. However, these probes have several limitations: poor control of interface's electrical environment and very fragile contacts. As integrated circuits become faster and more complex, the number of input/output pads increases

drastically. Therefore, the size and the spacing of the pads must be decreased. In order to achieve these requirements, there have been several attempts to fabricate probe structures with batch Si process [2-7]. The membrane probe card [2] is one of these attempts. Membrane probe cards offer many advantages over epoxy needle probe cards giving lower parasitic inductance, controlled impedance tips, and improved mechanical reliability. It combines tungsten probe tips and aluminum interconnects in the polyimide membrane formed on a silicon substrate. The major drawback of this technology is that additional air pressure is needed to supply sufficient, uniform contact forces to the probe tips. This becomes more problematic as chip complexity and the number of contacts increases. Another approach includes micro-cantilever probes that can be individually actuated [3]. An array of micro cantilevers actuated by bimorph heating are made for the wafer probe card, but it is very difficult for micro cantilevers to generate enough force to break the oxidized layer on the surface of the Al pad, and heater signal lines are needed in addition to the test signal lines.

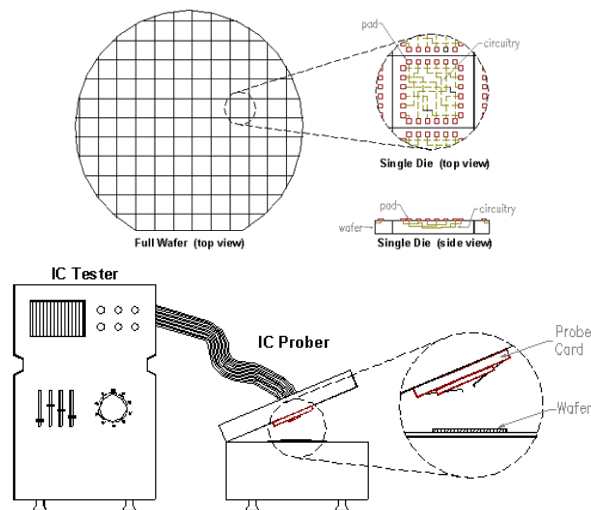


Fig. 1. Automatic test equipment.

In this paper, we have developed a novel silicon probe card using MEMS process in order to solve the limitation of fine pitch and high frequency, and problem of silicon process for probe card. This probe is applicable to less than 50  $\mu\text{m}$  of fine pitch, less than 5g of force, and higher than 2GHz of frequency.

## DESIGN & FABRICATION

Probe card design requirements can be divided into a variety of categories, one being mechanical and the other electrical performance. Mechanical performance can be divided into envelope, electromechanical, and performance. Electrical performance is also divided into contact quality, signal speed, and AC/DC signal quality [1]. In addition, the probing environment, probe card life, and the maintenance process are essential considerations. In this paper, we focused on planarity, compliance, overdrive, and force. Cantilever-type probe was fabricated with the following procedure as shown in Fig. 2. The starting material was 4 inch (100) Si wafer with the thickness of 525  $\mu\text{m}$ . A 50 nm thick epitaxial polysilicon was deposited on the Si wafer with patterned oxide at 1050  $^\circ\text{C}$  for 60 minutes [8].

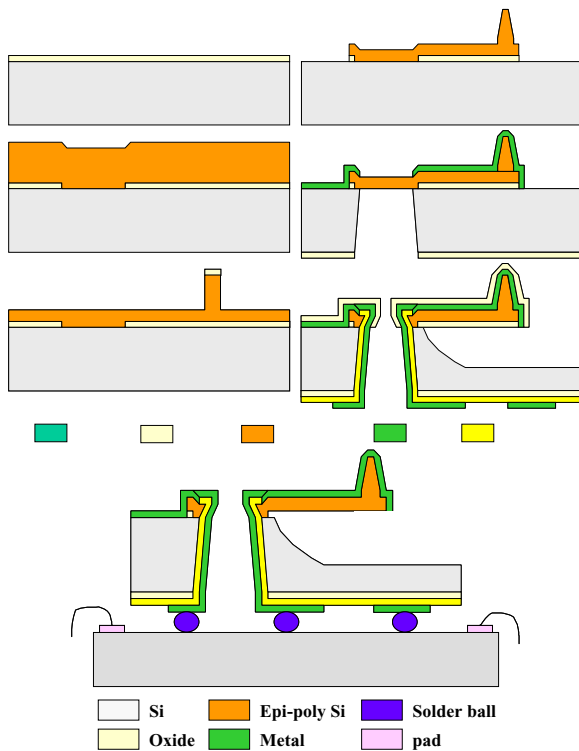


Fig. 2. Fabrication flow of epitaxial polysilicon probe process.

Firstly, a 4  $\mu\text{m}$  thick tetraethylorthosilicate (TEOS) was deposited on the back side to make through-hole, and etched by deep silicon RIE etcher after

patterning. Secondly, Ni was deposited by electroless process and Cu was deposited by electroplating. Finally, probe tips were formed after isotropic etching around cantilever using  $\text{XeF}_2$ . The fabricated probe array was 70  $\sim$  100  $\mu\text{m}$  of pitch and the etch depth under the probe was 50  $\mu\text{m}$ . To test the probing capability of the probe array, we tried to contact it on the Al pad and put the probe dies on PCB.

## RESULTS & DISCUSSION

A die with 64 pins probe tips was successfully fabricated as shown in Fig. 3 and attached on PCB. The mechanical characteristics of probe tips were measured using a manual machine. A small amount of tips were broken during tens of contact test, when we applied 4N  $\sim$  10N force which was much stronger than normal probing force. The probe marks, as shown in Fig. 4, were vivid in case of above force. After probe was deposited with Au, the contact resistance was less than 0.5  $\Omega$ .

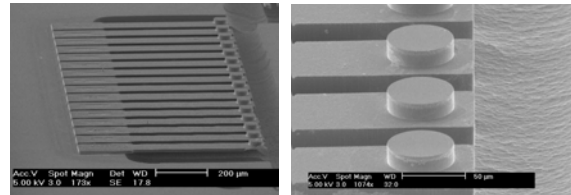


Fig. 3. 64 pins probe tips.

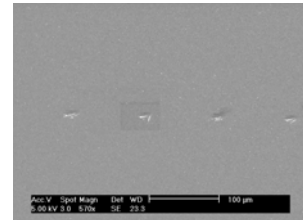


Fig. 4. Contact test on Al pads.

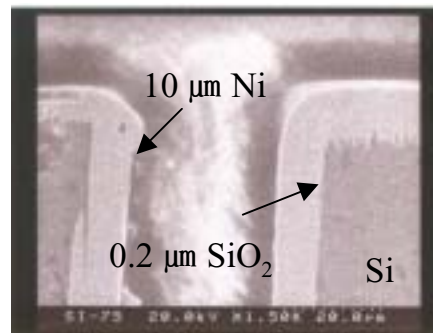


Fig. 5. Ni electroless plating through via holes.

To make fine pitch probe card, through-hole technology is essential. There have been several reports on the interconnection through holes [9-11]. S. Linder *et al.* demonstrated that through hole was formed by KOH wet etching, was electroplated by gold layer, and was

hermetically encapsulated subsequently [9]. The major drawback of this technology is that fine pitch process is impossible because of isotropic etching profile by KOH. Hyongsok T. Soh *et al.* showed another approach [10]. The through-wafer was etched by deep reactive ion etching system and aspect ratio was greater than 17:1. But this technology is needed special photoresist and has complicated process steps. Recently, Dong-Weon Lee *et al.* showed the advanced technology for through hole filling [11]. But this technology also has complex process steps.

In this paper, we used electroless and electro plating methods for interconnection. Electroless plating uses a redox reaction to deposit metal on an object without the passage of an electric current. Because it allows a constant metal ion concentration to bathe all parts of the object, it deposits metal evenly along edges, inside holes, and over irregularly shaped objects, which are difficult to plate evenly with electroplating. Electroless plating is also used to deposit a conductive surface on a nonconductive object to allow it to be electroplated. Electroless deposition is a technique for formation of metal thin films by reducing metal ions with reductant. The general processes of electroless plating are as follows; cleaning, etching, activation, acceleration, and electroless plating.

Table 1. Process for electroless Ni deposition.

Process type	Chemical Composition	Temp.	Time
Rinse	Distilled water	RT	1 min
Degreasing	10% acetone	RT	30 min
Alkali removal of fat	$\text{NH}_4\text{OH} : \text{H}_2\text{O}_2 : \text{H}_2\text{O} = 1 : 1 : 6$	70	10 min
Pickling	$\text{HCl} : \text{H}_2\text{O}_2 : \text{H}_2\text{O} = 1 : 1 : 5$	70	10 min
Etching	$\text{HF} : 1 (12\text{ml})$ $\text{NH}_4\text{F} : 6 (22.2\text{g}/50\text{ml})$	RT	10 sec
Catalyzing	$\text{PdCl}_2 : 0.1 \text{ g} / 200 \text{ ml}$ $\text{SnCl}_2 \cdot 2\text{H}_2\text{O} : 4 \text{ g} / 200 \text{ ml}$ $\text{HCl} : 16 \text{ ml} / 200 \text{ ml}$	45	7 min
Accelerating	10 % $\text{H}_2\text{SO}_4$	45	3 min
Basic plating composition	$\text{NiCl}_2 \cdot 6\text{H}_2\text{O} : 43.98 \text{ g} / \ell$ $\text{C}_6\text{H}_5\text{O}_7\text{Na}_3 \cdot 2\text{H}_2\text{O} : 58.82 \text{ g} / \ell$ $\text{NH}_4\text{Cl} : 50.01 \text{ g} / \ell$ $\text{NaH}_2\text{PO}_2 \cdot \text{H}_2\text{O} : 11.00 \text{ g} / \ell$ PH: variable pH adjusting substance : NaOH	variable	variable

The typical measured resistance of the through holes was between 0.01 and 0.3  $\Omega$  without contact to pads. To get the hole filled, electroless plating and electroplating is important together. First, in order to wash out for alkali and acid elements of the surface, we used two mixture liquids and dipped at 70°C after washing surface with 10% acetone for 30 minutes. One was 1:1:6(Vol %) =  $\text{NH}_4 : \text{H}_2\text{O}_2 : \text{D.I.}$  for alkali element,

and the other was 1:1:5(Vol %) =  $\text{HCl} : \text{H}_2\text{O}_2 : \text{D.I.}$  for acid element. Main electroless plating procedure was as shown in Table 1. Fig. 5 shows SEM photo of Ni electroless plating in the through via hole. The hole diameter was 50  $\mu\text{m}$  and the height of hole was 500  $\mu\text{m}$ . Finally, we electroplated via hole with Cu using electroplater (MDC Japan Co.). To achieve field test, the dies with probe tips were assembled on PCB. However, today's ATE is incongruent to adopt MEMS probe card because MEMS probe card is more fragile than epoxy-needle type probe card. Therefore, we consider that scramble PCB and interposer is needed to alleviate contact force at the tip. Fig. 6 shows the schematic of diagram for assembly.

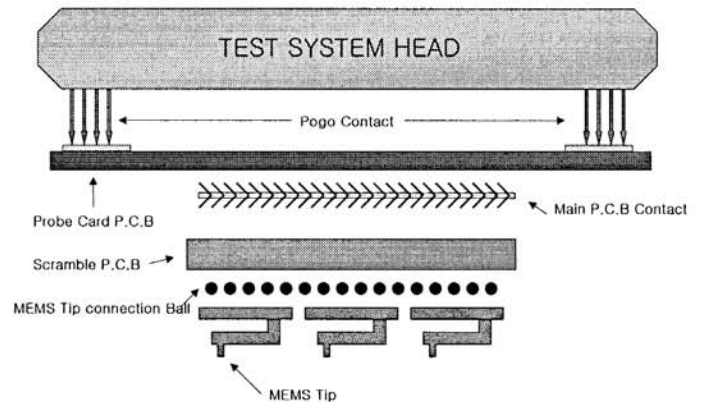


Fig. 6. A schematic diagram for assembly on PCB.

## CONCLUSION

In this paper, we have developed a novel cantilever-type probe card. To give more than 50  $\mu\text{m}$  of overdrive, we used epitaxial polysilicon for tip material. In addition, to make low contact resistance, we used nickel electroless plating and copper electroplating subsequently for metal. The characteristics of this probe, not shown in this paper, will be evaluated at the semiconductor company including mechanical performance and electrical performance such as DC/AC testing. This probe is suitable for wafer-level burn-in testing, function testing and circuit-board O/S testing. A combination of MEMS technology and conventional probe technology are helpful for next generation probe card. Since MEMS technology can support less than 50  $\mu\text{m}$  of fine pitch and 5g of force, and higher than 2 GHz bandwidths, most of probe card company try to adopt this technology. So far, silicon probe card, made with MEMS technology, has not qualified completely by field test such as mechanical and electrical test because tips have broken frequently under testing and life time have not proven yet. However, as MEMS based probe card is gradually improved, conventional epoxy-needle type probe card can be substituted in a few years.



## ACKNOWLEDGMENT

The authors would like to thank staffs of ISRC as well as fabrication manager of ISRC, Jong-jun Kim. This work was supported through CATS(Center for Advanced Transceiver System) by ministry of commerce, industry and energy on grant ISRC 2001-X-6140. And this work was partly funded through BK21(Brain Korea 21) by ministry of education.

## REFERENCES

- [1] R. D. Bates, "The search for the universal probe card solution", in the International Test Conference, Washington, DC, USA, Nov. 1997, pp533 – 538.
- [2] M. Beiley et al., "A micromachined array probe card – Fabrication process", IEEE Transaction on Components, Packaging, and Manufacturing Technology, Part B, Vol. 18, No. 1, pp179-183, Feb. 1995.
- [3] Yanwei Zhang, Yongxia Zhang, and R.B. Marcus, "Thermally actuated microprobes for a wafer probe card", IEEE Journal of Microelectromechanical Systems, Vol. 8, No. 1, March 1999, pp. 43-49.
- [4] Gong-seok Lee et al., "Fabrication of a bump-type Si probe card", in Microprocesses and Nanotechnology Conference, Tokyo, Japan, July 2000, pp76 –77.
- [5] Beth Pruitt et al., "Low force electrical contact measurements using piezoresistive MEMS cantilevers to thin-film metallization", in the 11<sup>th</sup> International Conference on Solid-State Sensors and Actuators (TRANSDUCERS'01, EUROSENSORS XV), Munich, Germany, June, 2001, pp1032-1035.
- [6] Toshihiro Itoh et al., "Characteristics of low force contact process for MEMS probe cards", in the 11<sup>th</sup> International Conference on Solid-State Sensors and Actuators (TRANSDUCERS'01, EUROSENSORS XV), Munich, Germany, June, 2001, pp222-225.
- [7] Sangjun Park et al., "High-yield Process for Fabricating Integrated Probes in Silicon for Micro-level Tip-height Uniformity", in Proceedings of SEMI Technical Symposium(STS): Innovation In Semiconductor Test, Assembly & Packaging, SEMI WEST 2001, San Jose, CA, USA, July 2001, pp81-88
- [8] Byeung-Leul Lee et al., "A Vacuum Packaged Differential Resonant Accelerometer using Electrostatic Stiffness Changing Effect" in 13th IEEE International Conference on Micro Electro Mechanical System, Miyazaki, Japan, Jan 2000, pp. 352 - 357
- [9] S. Linder et al., "Fabrication technology for wafer through-hole interconnections and three-dimensional stacks of chips and wafers", in the IEEE Workshop on Micro Electro Mechanical Systems(MEMS '94), Oiso, Japan, Jan. 1994, pp349 – 354.
- [10] Hyongsok T. Soh et al., "Ultra-low resistance, through-wafer via(TWV) technology and its application in three dimensional structures on silicon, Jpn. J. Appl. Phys. Vol. 38, Part 1, No. 4B, pp2393-2396, April 1999.
- [11] Dong-weon Lee et al., "Fabrication of microprobe array with sub-100nm nano-heater for nanometric thermal imaging and data storage", in the 14th IEEE International Conference on Micro Electro Mechanical Systems (MEMS '01), Interlaken, Switzerland, Jan. 2001, pp204 –207.